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SYSTEM AND METHOD FOR COMPENSATING FOR SUPPLY VOLTAGE INDUCED SIGNAL DELAY MISMATCHES

ABSTRACT OF THE DISCLOSURE

Various systems and methods providing signal delay compensation for circuits such as a multi-pair gigabit Ethernet transceiver are disclosed. In an analog implementation a buffer with an adjustable delay may be used to minimize the delay mismatch between clock trees. The delay of the adjustable-delay buffer is controlled by bias voltages that determine the charging and discharging current to the adjustable buffer. A phase detector circuit is used to compare the clock phases for rising and falling edges, and to adjust the bias voltages that control these edges. In a digital implementation a selector switch, responsive to a phase detector, may be used to route clock signals through circuit elements to delay clock signals.

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